IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO. LTD., Plaintiff, v. ON SEMICONDUCTOR CORP. and SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC, Defendants.	Civil Action No. ____________ **DEMAND FOR JURY TRIAL**

COMPLAINT

Plaintiff Samsung Electronics Co. Ltd. ("Samsung") for its Complaint against Defendants ON Semiconductor Corp. and Semiconductor Components Industries, LLC (collectively, "ON Semiconductor") hereby demands a jury trial and alleges as follows:

Parties

1. Plaintiff Samsung is a corporation organized under the laws of the Republic of Korea, having its principal place of business at Samsung Main Building, 250, Taepyun-ro 2-ka, Chung-ku, Seoul 100-742 Korea.

2. Samsung is in the business of manufacturing and selling a wide range of products. Specifically in relation to this action, Samsung manufactures and sells dynamic random access memories ("DRAMs").

3. On information and belief, Defendant ON Semiconductor Corp. is a Delaware corporation with its principal place of business at 5005 East McDowell Road, Phoenix, Arizona 85008.

4. On information and belief, Defendant Semiconductor Components Industries, LLC is a Delaware limited liability company with its principal place of business at 5005 East McDowell Road, Phoenix, Arizona 85008, is the principal domestic operating subsidiary of Defendant ON Semiconductor Corp, and does business under the name "ON Semiconductor."

Nature of Action

5. In this action, Samsung seeks a declaratory judgment of noninfringement and invalidity of three United States Patents pursuant to the Declaratory Judgment Act, 28 U.S.C. §§ 2201 and 2202, and the Patent Laws of the United States, 35 U.S.C. § 100 *et seq.*, and such other relief as this Court deems just and proper.

Jurisdiction and Venue

6. This Court has subject matter jurisdiction over the subject matter of this action under 28 U.S.C. §§ 2201-02 and 28 U.S.C. §§ 1331 and 1338(a).

7. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(b) and (c).

The Patents

8. U.S. Patent No. 5,563,594 (the "'594 patent") entitled "Circuit and Method of Timing Data Transfers" was filed on August 31, 1994 and issued on October 8, 1996. A Certificate of Correction issued on April 29, 1997. The inventors named on the '594 patent are

David K. Ford and Bernard E. Weir, III. A copy of the '594 patent is attached hereto as Exhibit A.

9. U.S. Patent No. 6,362,644 (the "'644 patent") entitled "Programmable Termination for Integrated Circuits" was filed on August 1, 2000 and issued on March 26, 2002. The inventors named on the '644 patent are Philip A. Jeffery and Stephen G. Shook. A copy of the '644 patent is attached hereto as Exhibit B.

10. U.S. Patent No. 5,361,001 (the "'001 patent") entitled "Circuit and Method of Previewing Analog Trimming" was filed on December 3, 1993 and issued on November 1, 1994. The inventor named on the '001 patent is David L. Stolfa. A copy of the '001 patent is attached hereto as Exhibit C.

11. On information and belief, ON Semiconductor owns the '594, '644, and '001 patents and has the right to sue for infringement.

Count I
(Declaratory Judgment Action for a Declaration of
<u>Noninfringement and Invalidity of U.S. Patent No. 5,563,594)</u>

12. Paragraphs 1 through 11 are incorporated by reference as if stated fully herein.

13. ON Semiconductor has accused Samsung of infringing the '594 patent through its manufacture, sale, use, and/or importation of certain DRAMs.

14. ON Semiconductor has demanded that Samsung license the '594 patent for exorbitant sums of money, and has informed Samsung that it will not go away unless Samsung enters into a patent license with ON Semiconductor.

15. Samsung has informed ON Semiconductor that it will not pay ON Semiconductor the exorbitant sums that it is seeking, and has a reasonable apprehension that ON Semiconductor will file a patent infringement action against Samsung for infringement of the '594 patent if

Samsung continues to manufacture, sell use, and/or import certain of its DRAMs. A valid and justiciable controversy has arisen and exists between Samsung and ON Semiconductor within the meaning of 28 U.S.C. § 2201.

16. Samsung has not directly or indirectly infringed any valid and enforceable claim of the '594 patent, either literally or under the doctrine of equivalents.

17. The '594 patent is invalid because of its failure to comply with one or more of the requirements of the patent laws of the United States, including, without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

18. A judicial declaration of noninfringement and invalidity is necessary and appropriate in order to resolve this controversy.

Count II
(Declaratory Judgment Action for a Declaration of
Noninfringement and Invalidity of U.S. Patent No. 6,362,644)

19. Paragraphs 1 through 18 are incorporated by reference as if stated fully herein.

20. ON Semiconductor has accused Samsung of infringing the '644 patent through its manufacture, sale, use, and/or importation of certain DRAMs.

21. ON Semiconductor has demanded that Samsung license the '644 patent for exorbitant sums of money, and has informed Samsung that it will not go away unless Samsung enters into a patent license with ON Semiconductor.

22. Samsung has informed ON Semiconductor that it will not pay ON Semiconductor the exorbitant sums that it is seeking, and has a reasonable apprehension that ON Semiconductor will file a patent infringement action against Samsung for infringement of the '644 patent if Samsung continues to manufacture, sell use, and/or import certain of its DRAMs. A valid and

justiciable controversy has arisen and exists between Samsung and ON Semiconductor within the meaning of 28 U.S.C. § 2201.

23. Samsung has not directly or indirectly infringed any valid and enforceable claim of the '644 patent, either literally or under the doctrine of equivalents.

24. The '644 patent is invalid because of its failure to comply with one or more of the requirements of the patent laws of the United States, including, without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

25. A judicial declaration of noninfringement and invalidity is necessary and appropriate in order to resolve this controversy.

Count III
(Declaratory Judgment Action for a Declaration of
Noninfringement and Invalidity of U.S. Patent No. 5,361,001)

26. Paragraphs 1 through 25 are incorporated by reference as if stated fully herein.

27. ON Semiconductor has accused Samsung of infringing the '001 patent through its manufacture, sale, use, and/or importation of certain DRAMs.

28. ON Semiconductor has demanded that Samsung license the '001 patent for exorbitant sums of money, and has informed Samsung that it will not go away unless Samsung enters into a patent license with ON Semiconductor.

29. Samsung has informed ON Semiconductor that it will not pay ON Semiconductor the exorbitant sums that it is seeking, and has a reasonable apprehension that ON Semiconductor will file a patent infringement action against Samsung for infringement of the '001 patent if Samsung continues to manufacture, sell use, and/or import certain of its DRAMs. A valid and justiciable controversy has arisen and exists between Samsung and ON Semiconductor within the meaning of 28 U.S.C. § 2201.

30. Samsung has not directly or indirectly infringed any valid and enforceable claim of the '001 patent, either literally or under the doctrine of equivalents.

31. The '001 patent is invalid because of its failure to comply with one or more of the requirements of the patent laws of the United States, including, without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

32. A judicial declaration of noninfringement and invalidity is necessary and appropriate in order to resolve this controversy.

Prayer for Relief

WHEREFORE, Samsung prays for judgment as follows:

A. That it be declared that Samsung has not directly or indirectly infringed any claims of U.S. Patent Nos. 5,563,594, 6,362,644, and 5,361,001 under any subsection of 35 U.S.C. § 271;

B. That it be declared that U.S. Patent Nos. 5,563,594, 6,362,644, and 5,361,001 are invalid;

C. That Samsung be awarded its costs and disbursements in this action, including reasonable attorneys' fees; and

D. That Samsung be awarded such other and further relief as the Court deems just and proper.

JURY DEMAND

Samsung demands a trial by jury on all issues triable of right by a jury.

Respectfully submitted,

Dated: November 30, 2006

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EXHIBIT A

US005563594A

United States Patent [19]

Ford et al.

[11] Patent Number: 5,563,594

[45] Date of Patent: Oct. 8, 1996

[54] CIRCUIT AND METHOD OF TIMING DATA TRANSFERS

[75] Inventors: **David K. Ford**, Gilbert; **Bernard E. Weir, III**, Chandler, both of Ariz.

[73] Assignee: **Motorola**, Schaumburg, Ill.

[21] Appl. No.: **298,715**

[22] Filed: **Aug. 31, 1994**

[51] Int. Cl.[6] **H03M 9/00**

[52] U.S. Cl. **341/100**; 341/101; 327/279

[58] Field of Search 341/100, 101; 326/93; 327/160, 175, 265, 279

[56] **References Cited**

U.S. PATENT DOCUMENTS

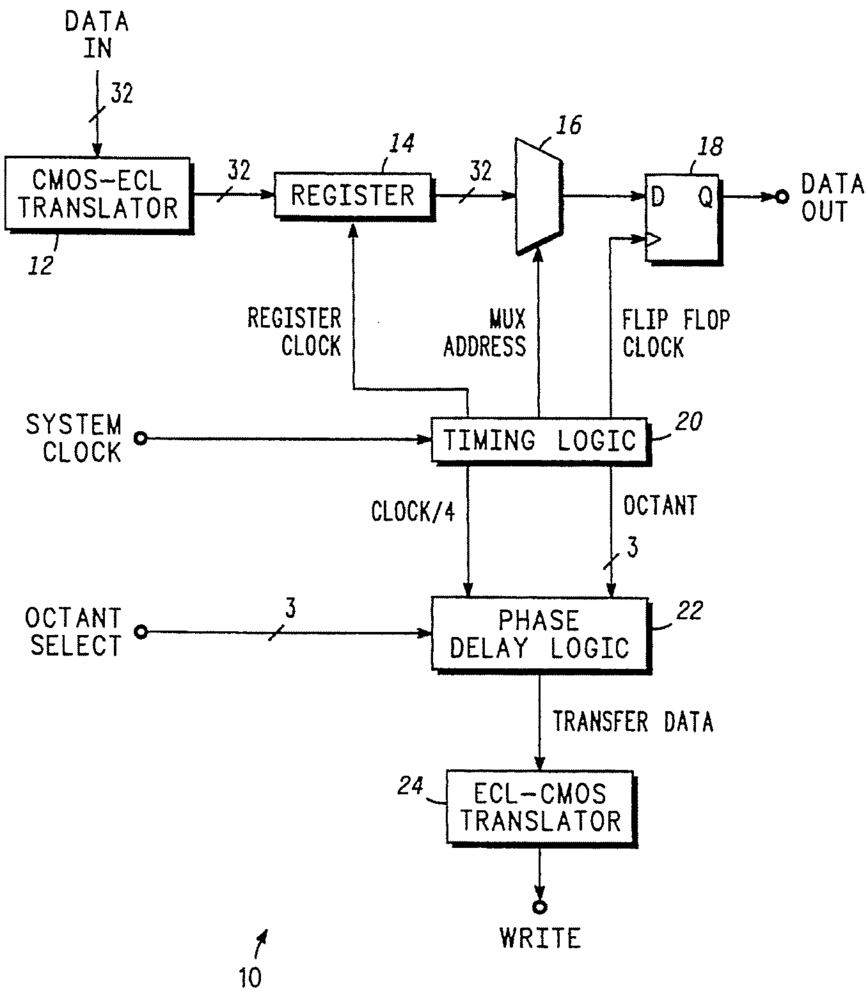
4,218,758	8/1980	Allen et al.	364/900
4,445,215	4/1984	Svendsen	370/279
4,815,107	3/1989	Kishimoto et al.	375/96
5,379,038	1/1995	Matsumoto	341/101

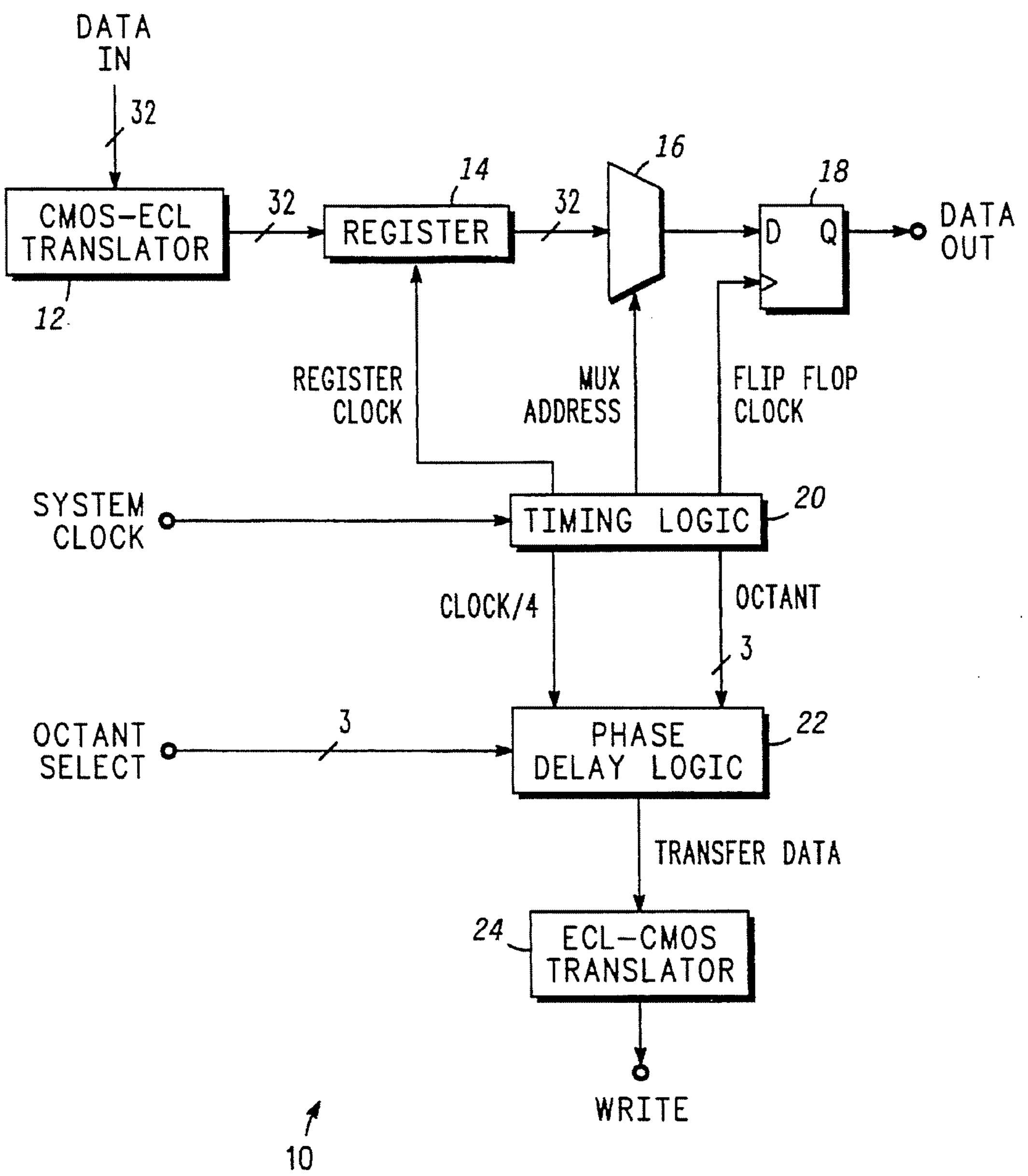
Primary Examiner—Marc S. Hoff
Attorney, Agent, or Firm—Robert D. Atkins

[57] **ABSTRACT**

A data conversion circuit receives input data from external sourcing logic and performs a parallel-serial conversion. Likewise, a data conversion circuit performs a serial-parallel conversion and presents output data to external sinking logic. In the parallel-serial conversion (**10**), the input data is translated (**12**) and stored in a register (**14**). A multiplexer (**16**) rotates through the data to provide the serial output. In the serial-parallel conversion (**70**), the input data is sequenced into a multiplexer (**74**) to achieve the parallel data word. The parallel data word is stored in a register (**76**) before presenting it to external logic. Phase delay logic (**22**) sets the delay of a transfer data control signal that requests data be read or written. Once the proper delay is determined by experimentation, the phase delay logic controls the phase of the transfer data control signal to request more data at the correct time, or present more data at the correct time, to allow maximum operating speed for the data converter.

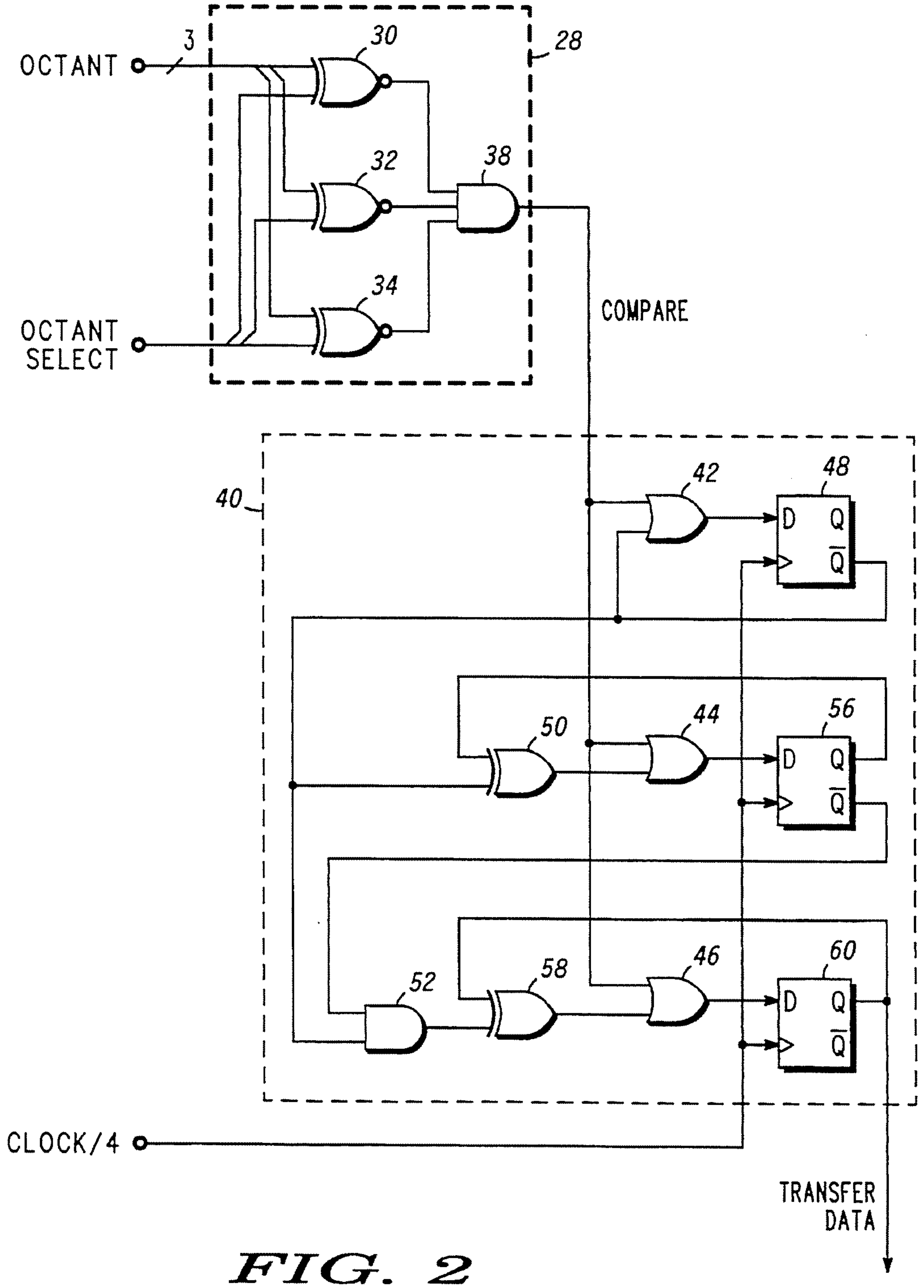
19 Claims, 3 Drawing Sheets





DATA IN
32
CMOS-ECL TRANSLATOR
12
32
14
REGISTER
32
16
18
D Q
DATA OUT
REGISTER CLOCK
MUX ADDRESS
FLIP FLOP CLOCK
SYSTEM CLOCK
TIMING LOGIC
20
CLOCK/4
OCTANT
3
OCTANT SELECT
3
PHASE DELAY LOGIC
22
TRANSFER DATA
24
ECL-CMOS TRANSLATOR
WRITE
10

FIG. 1



OCTANT
3
30
28
32
38
34
OCTANT
SELECT
COMPARE
40
42
48
D
Q
Q̄
50
44
56
52
58
46
60
CLOCK/4
TRANSFER
DATA

FIG. 2

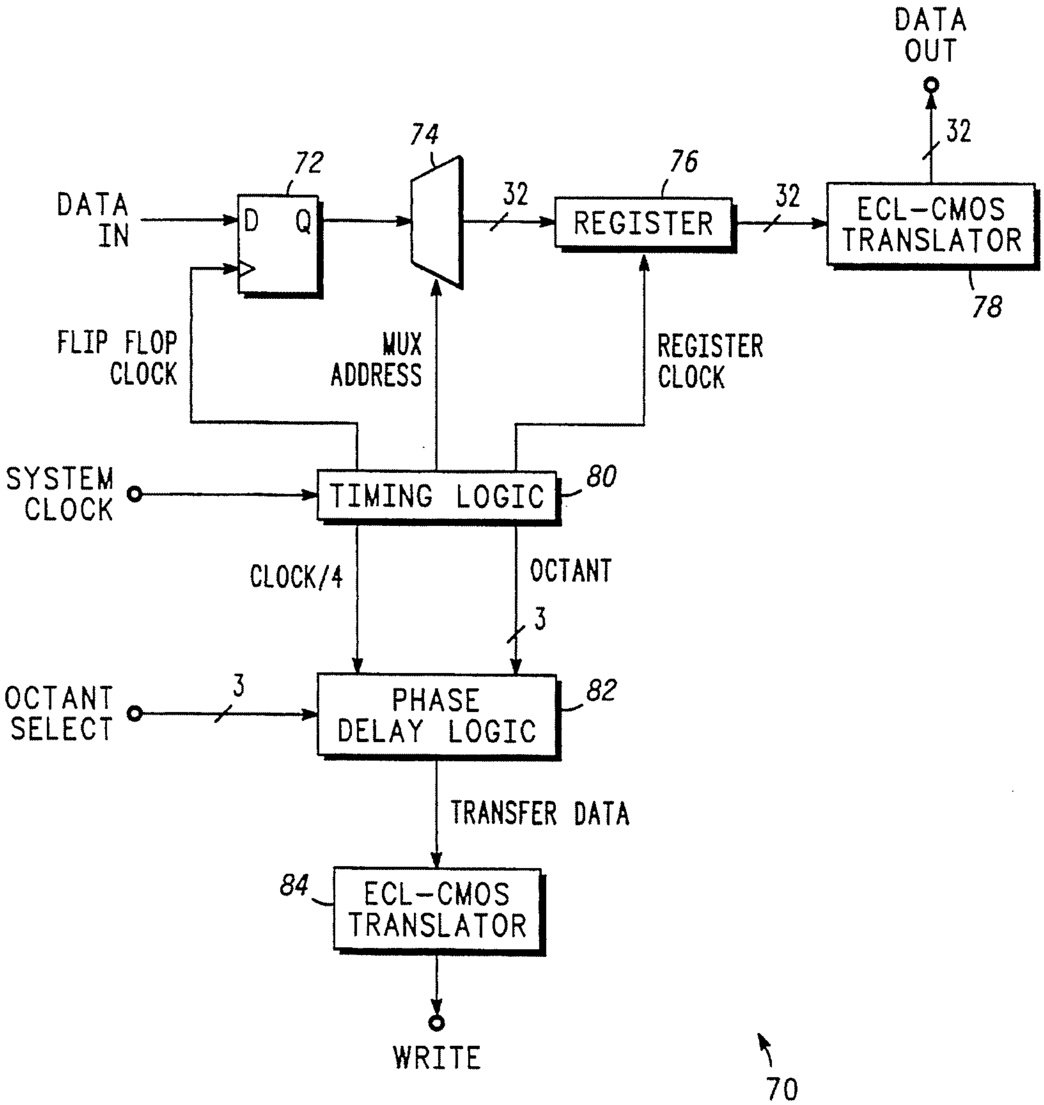

DATA OUT
32
72
74
76
DATA IN
D
Q
32
REGISTER
32
ECL-CMOS TRANSLATOR
78
FLIP FLOP CLOCK
MUX ADDRESS
REGISTER CLOCK
SYSTEM CLOCK
TIMING LOGIC
80
CLOCK/4
OCTANT
3
OCTANT SELECT
3
PHASE DELAY LOGIC
82
TRANSFER DATA
84
ECL-CMOS TRANSLATOR
WRITE
70

FIG. 3

CIRCUIT AND METHOD OF TIMING DATA TRANSFERS

BACKGROUND OF THE INVENTION

The present invention relates in general to digital timing circuits and, more particularly, to controlling the phase of a data transfer signal to set the proper timing for reading or writing to a data register.

Parallel-serial converters are commonly used in digital circuit design to convert multi-bit signals to a string of data bits that are serially transmitted one at a time. Serial-parallel converters in turn convert the string of data bits back to multi-bit signals. In both applications, a data register is typically embedded within an integrated circuit that periodically receives new data sourced by external logic, or sources new data for external logic. Timing generation logic for reading or writing the data register is also embedded within the integrated circuit. The timing generation logic asserts a periodic signal to the external logic requesting data be presented to or removed from the data register.

Many applications involve high speed operation, say in the gigahertz range. The data transaction must be completed within a predetermined time period. That is, write data must be present and valid for a setup time before, and hold time after it is loaded into the register by a clock signal. Likewise, read data must be present and valid for a setup time before, and hold time after it is read by external logic. Unfortunately at such high data rates, the propagation delay uncertainties of the external logic are almost as long as the entire transaction period.

When the periodic signal is asserted to the external logic, requesting that new data be read or written, the external logic begins the time-consuming process of retrieving or storing new data. In the case of a request from the IC to the external logic to write new data, when the external logic finally presents new data to the integrated circuit, the new data typically propagates through buffer logic and eventually reaches the data register. The internal timing generation logic asserts a clock signal to load the data register. When the data transaction is so fast that propagation delay uncertainties consume almost the entire time period, there is no assurance that data arrives at the data register within register setup and hold-time constraints.

Since the write data register and timing logic are embedded within the integrated circuit, it is difficult to directly measure the actual write setup and hold-time. That is, the setup and hold-time are not readily observable by the external logic. If the write data setup and hold-time are unknown, the data rate of the external sourcing logic must be reduced to ensure sufficient setup and hold-time. Otherwise, where the propagation time uncertainty consumes a large portion of the transaction time period, the data transaction may fail to correctly time the data transfer under a worst-case timing analysis.

Hence, a need exists to properly set the timing of requesting more write data or read data for the data register to achieve maximum data transfer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram illustrating a parallel-serial converter;

FIG. **2** is a schematic diagram illustrating the phase delay logic of FIG. **1**; and

FIG. **3** is a block diagram illustrating a serial-parallel converter.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. **1**, a parallel-serial converter **10** is shown suitable for manufacturing as an integrated circuit using conventional integrated circuit processes. A CMOS-ECL voltage translator circuit **12** receives a 32-bit DATA IN word from external sourcing logic (not shown) operating at CMOS logic levels. CMOS-ECL voltage translator circuit **12** provides a 32-bit signal operating at ECL logic levels to 32-bit register **14**. Register **14** loads data at rising edge of a REGISTER CLOCK signal. Multiplexer **16** rotates through the individual bit locations of register **14** under control of the MUX ADDRESS signal and provides serial bits to the data input of flipflop **18**. Flipflop **18** transfers the serial data signal to DATA OUT at its Q-output upon receiving a FLIPFLOP CLOCK signal.

Timing logic **20** operates in response to a SYSTEM CLOCK signal, running for example at 2.5 gigahertz, for providing the FLIPFLOP CLOCK signal and the REGISTER CLOCK signal. The FLIPFLOP CLOCK signal operates in phase and at the same frequency as the SYSTEM CLOCK. The REGISTER CLOCK signal is derived from dividing the SYSTEM CLOCK by value thirty-two. The REGISTER CLOCK signal is aligned on the same rising edge as the SYSTEM CLOCK. The MUX ADDRESS is reset to zero with each REGISTER CLOCK and counts up with the SYSTEM CLOCK to value thirty-two. Thus, the serialized data stream DATA OUT is sent at the SYSTEM CLOCK frequency with the duration of each serial bit time the same as the period of the SYSTEM CLOCK.

Timing logic **20** further provides a CLOCK/4 signal and a 3-bit OCTANT signal. The CLOCK/4 signal is derived by dividing the SYSTEM CLOCK by value four with alignment on the rising edges of SYSTEM CLOCK. The OCTANT signal takes one of eight binary encoded values (0 through 7) as seen in Table 1. During a first group of four consecutive SYSTEM CLOCKS C0–C3, OCTANT has a value "000". During the second group of four consecutive SYSTEM CLOCKS C4–C7, OCTANT has a value "001", and so on. The OCTANT signal changes state at each rising edge of CLOCK/4, for example, by incrementing a counter (not shown). Timing logic **20** includes combinational logic to divide the SYSTEM CLOCK and reset the MUX ADDRESS signal. Such combinational logic can be implemented from the aforedescribed operations.

TABLE 1

SYSTEM CLOCK	OCTANT
C0–C3	"000"
C4–C7	"001"
C8–C11	"010"
C12–C15	"011"
C16–C19	"100"
C20–C23	"101"
C24–C27	"110"
C28–C31	"111"

Phase delay logic circuit **22** receives CLOCK/4 and OCTANT signals from timing logic **20**, and an OCTANT SELECT signal from the external logic (not shown). ECL-CMOS translator **24** converts the TRANSFER DATA signal from phase delay logic circuit **22** to CMOS logic levels for the external logic. Upon receiving the WRITE control

signal, the external logic sends the next 32-bit DATA IN word.

It is important for the overall circuit operation that the output signal from REGISTER **14** does not become metastable. The 32-bit data at the output of translator circuit **12** must be stable for a finite "setup time" before the rising edge of REGISTER CLOCK. Likewise, the 32-bit data must remain stable for a finite "hold-time" after the rising edge of REGISTER CLOCK to ensure that register **14** clocks in valid data. Any violation of setup and hold-time may cause the register output to become metastable, yielding indeterminate logic levels for an indeterminate time duration.

Accordingly, as a feature of the present invention, phase delay logic circuit **22** sets the timing of TRANSFER DATA signal by altering its phase as programmed by the 3-bit OCTANT SELECT signal to request more data at the proper time to allow parallel-serial converter **10** to complete processing the previous data. In practice during a calibration sequence, the OCTANT SELECT signal may be set to various values to determine proper delay time necessary before the WRITE is asserted so that the next DATA IN word arrives at the optimum time to ensure proper data set-up and hold times at the input of register **14** and to allow time to complete processing the previous data. Once the proper delay is determined by experimentation, phase delay logic circuit **22** asserts the TRANSFER DATA signal at the correct time by controlling its phase to allow maximum operating speed for parallel-serial converter **10** given the required set-up and hold-time of register **14**.

Turning to FIG. **2**, further detail of phase delay logic circuit **22** is shown including a digital comparator **28** implemented as exclusive-NOR (XNOR) gates **30**, **32** and **34** and AND gate **38**. XNOR gate **30** receives bit**0** of the OCTANT signal and bit**0** of the OCTANT SELECT signal. XNOR gate **32** receives bit**1** of the OCTANT signal and bit**1** of the OCTANT SELECT signal. XNOR gate **34** receives bit**2** of the OCTANT signal and bit**2** of the OCTANT SELECT signal. The outputs of XNOR gates **32–36** are coupled to inputs of AND gate **38**. If the OCTANT signal matches the OCTANT SELECT signal, AND gate **38** receives all logic ones and provides a logic one COMPARE signal. Otherwise, the COMPARE signal from AND gate **38** is logic zero.

Logic block **40** provides a symmetric 50% duty cycle for the TRANSFER DATA signal by counting down after the COMPARE signal sets the TRANSFER DATA (most significant bit of three bit down-counter) to logic one. The COMPARE signal from AND gate **38** is applied to first inputs of OR gates **42**, **44** and **46**. The output of OR gate **42** is coupled to the D-input of flipflop **48**. The $\overline{Q}$-output of flipflop **48** is coupled to the second input of OR gate **42**, to an input of exclusive-OR (XOR) gate **50**, and to an input of AND gate **52**. The output of XOR gate **50** is coupled to a second input of OR gate **44** that in turn has an output coupled to the D-input of flipflop **56**. The Q-output of flipflop **56** is coupled to the second input of XOR gate **50**, while the $\overline{Q}$-output of flipflop **56** is coupled to the second input of AND gate **52**. The output of AND gate **52** is coupled to a first input of XOR gate **58** that in turn has an output coupled to the second input of OR gate **46**. The output of OR gate **46** is coupled to the D-input of flipflop **60**. The Q-output of flipflop **60** is coupled to the second input of XOR gate **58** and further provides the TRANSFER DATA signal to ECL-CMOS translator **24** in FIG. **1**. Flipflops **48**, **56** and **60** receive the CLOCK/4 signal at their clock inputs.

During the 32-bit parallel to serial conversion, the 3-bit OCTANT signal increments on every rising edge of CLOCK/4, i.e. every four SYSTEM CLOCKS. When the 3-bit OCTANT signal matches the externally-supplied 3-bit OCTANT SELECT signal, the COMPARE signal is asserted as logic one. The Q-outputs of flipflops **48**, **56** and **60** go to logic one on the next rising edge of the CLOCK/4 signal. The TRANSFER DATA signal goes to logic one. When the OCTANT signal increments to its next value and COMPARE returns to logic zero, flipflops **48**, **56** and **60** operate as a 3-bit synchronous down counter and decrement with each rising edge of CLOCK/4. Since the TRANSFER DATA signal is the most significant bit of the down counter, it remains logic one for the first half of the counts and returns to logic zero for the second half of the counts. Logic block **40** thus provides a symmetric 50% duty cycle for the TRANSFER DATA signal.

For example, assume that the 32-bit DATA IN signal is latched into register **14** by the REGISTER CLOCK. In the present example, it has been determined by experimentation that the OCTANT SELECT signal "001" sets the proper phase delay before asserting TRANSFER DATA to the external logic to send the next DATA IN word. The delay determines the amount of time parallel-serial converter **10** needs to complete processing the present data word and be ready for the next. Assume that the Q-outputs of the flipflops begin at logic one and the $\overline{Q}$-outputs begin as logic zero. The first four SYSTEM CLOCKS **C0–C3** correspond to multiplexer **16** reading the four least significant bits D**0**–D**3** from register **14**. At the first rising edge of CLOCK/4 (clock **C0**), the OCTANT signal is "**000**" and does not match the OCTANT SELECT signal "001". Consequently, the COMPARE signal is logic zero.

At the second rising edge of CLOCK/4 (clock C4), the OCTANT signal switches to "001" and matches the OCTANT SELECT signal causing the COMPARE signal goes to logic one. The outputs of OR gates **42–46** go to logic one due to the logic one COMPARE signal for the initial state of the down count. Four SYSTEM CLOCKS later, the third rising edge of CLOCK/4 (clock C8) clocks the logic ones into flipflops **48**, **56** and **60** and sets their Q-outputs to logic one. The OCTANT signal switches to "010" and no longer matches the OCTANT SELECT signal. The COMPARE signal returns to logic zero. XOR gate **50** receives a logic zero from the $\overline{Q}$-output of flipflop **48** and a logic one from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic one. The D-input of flipflop **56** receives a logic one from OR gate **44**. AND gate **52** receives logic zeroes from flipflops **48** and **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The fourth rising edge of CLOCK/4 (clock C12) sets the $\overline{Q}$-output of flipflop **48** to logic one while the Q-outputs of flipflops **56** and **60** remain logic one. The output of OR gate **42** goes to logic one. XOR gate **50** receives a logic one from the $\overline{Q}$-output of flipflop **48** and a logic one from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic zero. The D-input of flipflop **56** receives a logic zero from OR gate **44**. AND gate **52** receives a logic one from flipflop **48** and a logic zero from flipflop **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The fifth rising edge of CLOCK/4 (clock C16) sets the Q-outputs of flipflops **48** and **60** to logic one while the Q-output of flipflop **56** goes to logic zero. The output of OR gate **42** goes to logic zero. XOR gate **50** receives logic zeroes from the $\overline{Q}$-output of flipflop **48** and the Q-output of

flipflop **56** and sets the second input of OR gate **44** to logic zero. The D-input of flipflop **56** receives a logic zero from OR gate **44**. AND gate **52** receives a logic zero from flipflop **48** and a logic one from flipflop **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The sixth rising edge of CLOCK/4 (clock **C20**) sets the $\overline{Q}$-outputs of flipflops **48** and **56** to logic one while the Q-output of flipflop **60** remains logic one. XOR gate **50** receives a logic one from the $\overline{Q}$-output of flipflop **48** and a logic zero from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic one. The D-input of flipflop **56** receives a logic one from OR gate **44**. AND gate **52** receives logic ones from flipflops **48** and flipflop **56**. XOR gate **58** receives a logic one from AND gate **52** and a logic one from flipflop **60** and provides a logic zero to OR gate **46**. The D-input of flipflop **60** goes to logic zero.

The seventh rising edge of CLOCK/4 (clock **C24**) sets the TRANSFER DATA signal to logic zero. The TRANSFER DATA signal remains logic zero for the next four CLOCK/4 cycles, i.e. **C24–C31** and **C0–C7**, as the down counter completes the second half of its count down sequence. Logic **40** thus provides a symmetric 50% duty cycle. Either edge of the TRANSFER DATA signal may be used to trigger the external logic to send more data to parallel-serial converter **10**. By controlling the phase of TRANSFER DATA, the correct timing is established for data transfer so that the requested data arrives at the optimum time to maximize the operating speed of parallel-serial converter **10**.

The aforedescribed phase control over the TRANSFER DATA is equally applicable to serial-parallel conversion such as shown in FIG. **3**. Serial-parallel converter **70** is shown suitable for manufacturing as an integrated circuit using conventional integrated circuit processes. The data input of flipflop **72** receives the serial DATA IN signal from external sourcing logic (not shown) and passes it to multiplexer **74** at each FLIPFLOP CLOCK. Multiplexer **74** rotates through its individual bit locations under control of the MUX ADDRESS signal and provides parallel bits to register **76**. Register **76** loads data at rising edge of a REGISTER CLOCK signal. A CMOS-ECL voltage translator circuit **78** converts the 32-bit data word from register **76** to CMOS logic levels.

Timing logic **80** operates in response to a SYSTEM CLOCK signal, operating for example at 2.5 gigahertz, for providing the FLIPFLOP CLOCK signal and the REGISTER CLOCK signal. The FLIPFLOP CLOCK signal operates in phase and at the same frequency as the SYSTEM CLOCK. The REGISTER CLOCK signal are derived from dividing the SYSTEM CLOCK by value thirty-two. The REGISTER CLOCK signal is aligned on the same rising edge as the SYSTEM CLOCK. The MUX ADDRESS is reset to zero with each REGISTER CLOCK and counts up with the SYSTEM CLOCK to value thirty-two. Thus, the serialized data stream DATA OUT is sent at the SYSTEM CLOCK frequency with the duration of each serial bit time the same as the period of the SYSTEM CLOCK. Timing logic **20** further provides a CLOCK/4 signal and a 3-bit OCTANT signal. The CLOCK/4 signal is derived by dividing the SYSTEM CLOCK by value four aligned with the rising edges of SYSTEM CLOCK. The OCTANT signal takes one of eight binary encoded values (0 through 7) as seen in Table 1. Timing logic **80** includes combinational logic to divide the SYSTEM CLOCK and reset the MUX ADDRESS signal. Such combinational logic can be implemented from the aforedescribed operations.

Phase delay logic circuit **82** receives CLOCK/4 and OCTANT signals from timing logic **80**, and an OCTANT SELECT signal from external logic (not shown). ECL-CMOS translator **84** converts the TRANSFER DATA signal from phase delay logic circuit **82** to CMOS logic levels for the external logic. Upon receiving the WRITE control signal, the external logic sends the next DATA IN bit. Phase delay logic circuit **82** follows the same description given in FIG. **2** and asserts the TRANSFER DATA signal at the correct time to allow maximum operating speed for serial-parallel converter **70** given the required set-up and hold-time of register **76**.

By now it should be appreciated that the present invention provides proper timing of the data transfer between external data sourcing or sinking logic and data conversion circuits. Phase delay logic sets the delay for a transfer data control signal as programmed by a select signal. During a calibration sequence, the select signal is set to various values to determine proper delay time necessary before requesting that more data be read or written. Once the proper delay is determined by experimentation, the phase delay logic circuit asserts the transfer data signal at the correct time by controlling its phase, to allow maximum operating speed for the data conversion given the required set-up and hold-time of the embedded register and of the external logic. By controlling the phase of transfer data requests, the correct timing is established to ensure proper data set-up and hold times and to allow complete processing before the next data word needs to be read or written.

While specific embodiments of the present invention have been shown and described, further modifications and improvements will occur to those skilled in the art. It is understood that the invention is not limited to the particular forms shown and it is intended for the appended claims to cover all modifications which do not depart from the spirit and scope of this invention. The present invention is applicable to other types of data processing circuits that must control timing of incoming data.

What is claimed is:

1. A phase delay circuit, comprising:

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal for counting down to generate an output signal having a symmetric duty cycle.

2. The circuit of claim **1** wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

3. The circuit of claim **2** wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said

compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

4. The circuit of claim 3 wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

5. The circuit of claim 4 wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

6. The circuit of claim 5 wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

7. A method of selecting phase delay of a transfer data control signal, comprising the steps of:

comparing first and second control signals and generating a compare signal having a first state when said first and second control signals match; and

initializing a count value in response to said compare signal; and

counting down said count value in response to a clock signal to provide a most significant bit of said count value with a symmetric duty cycle.

8. A data conversion circuit, comprising:

a register having an input coupled for receiving parallel input data and having an output;

a multiplexer having an input coupled to said output of said register for providing serial data;

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal for counting down to generate a transfer data signal having a symmetric duty cycle to enable transfer of said parallel input data to said register.

9. The circuit of claim 8 wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

10. The circuit of claim 9 wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

11. The circuit of claim 10 wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

12. The circuit of claim 11 wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

13. The circuit of claim 12 wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

14. A data conversion circuit, comprising:

a multiplexer having an input coupled for receiving serial input data and having an output;

a register having an input coupled to said output of said register for providing prarllel data;

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal having a symmetric duty cycle to enable transfer of said serial input data to said register.

15. The circuit of claim 14 wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

16. The circuit of claim 15 wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

17. The circuit of claim 161wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

18. The circuit of claim 17 wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

19. The circuit of claim 18 wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,563,594

DATED : October 8, 1996

INVENTOR(S) : David K. Ford et al.

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

In claim 14, column 9, line 30, insert --for counting down to generate a transfer data signal-- after "signal".

In claim 17, column 10, line 7, delete "161wherein" and insert --16 wherein--.

Signed and Sealed this

Twenty-ninth Day of April, 1997

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

EXHIBIT B

US006362644B1

(12) **United States Patent**
Jeffery et al.

(10) **Patent No.: US 6,362,644 B1**
(45) **Date of Patent: Mar. 26, 2002**

(54) **PROGRAMMABLE TERMINATION FOR INTEGRATED CIRCUITS**

(75) Inventors: **Philip A. Jeffery**, Tempe; **Stephen G. Shook**, Gilbert, both of AZ (US)

(73) Assignee: **Semiconductor Components Industries LLC**, Phoenix, AZ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/630,090**

(22) Filed: **Aug. 1, 2000**

(51) **Int. Cl.**[7] **H03K 17/16**
(52) **U.S. Cl.** **326/30**; 326/101
(58) **Field of Search** 326/30, 62, 63, 326/101; 327/333, 564, 565

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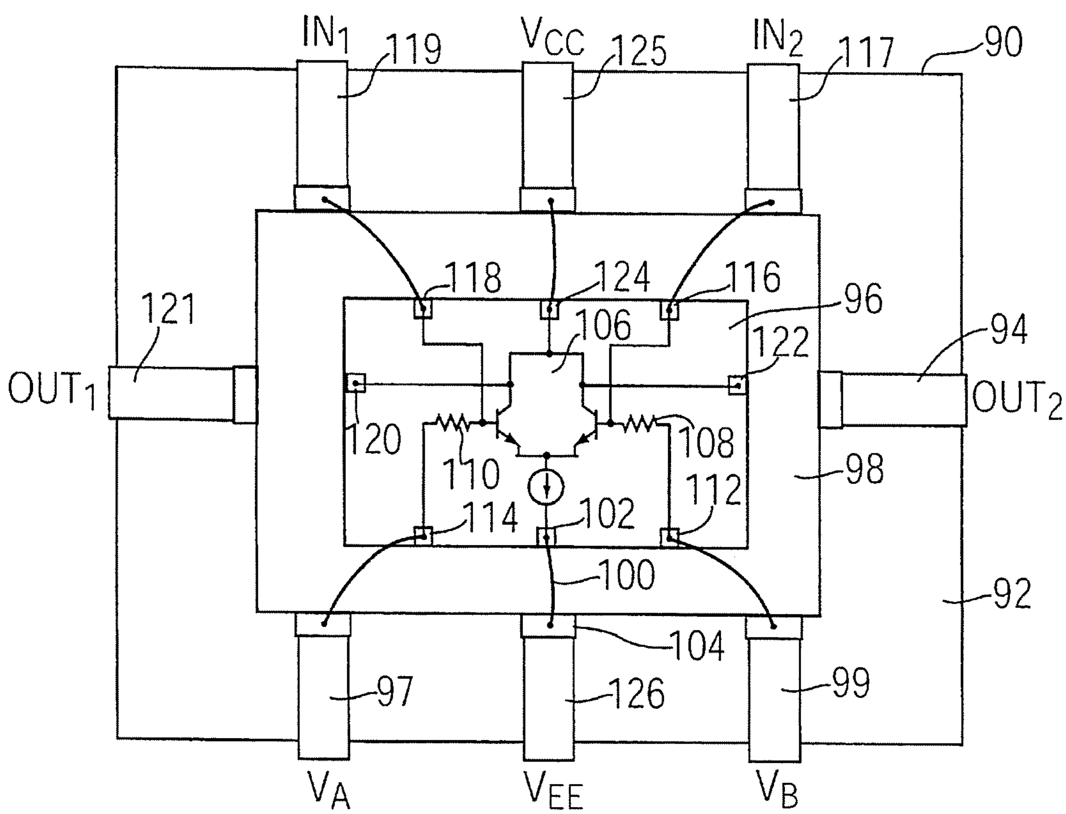
Primary Examiner—Tuan T. Lam

(57) **ABSTRACT**

A receiver circuit (**16**) is programmable to operate with different logic family driver circuits (**10**). The receiver circuit has two external configuration pins (**22**,) **24**) that are configured to provide the necessary termination for the type of logic family driver circuit used. To terminate the receiver circuit (**16**) for an ECL application will require first and second configuration pins (**22**,**24**) are connected to V_{CC}—2 volts. To terminate the receiver circuit (**16**) for a CML application will require the first configuration pin (**22**) and the second configuration pin (**24**) are connected to V_{CC}. LVDS termination for the receiver circuit (**16**) requires the first configuration pin (**22**) and the second configuration pin (**24**) are connected together. The configuration pins are external to a semiconductor package (**14**) housing the receiver circuit.

16 Claims, 3 Drawing Sheets



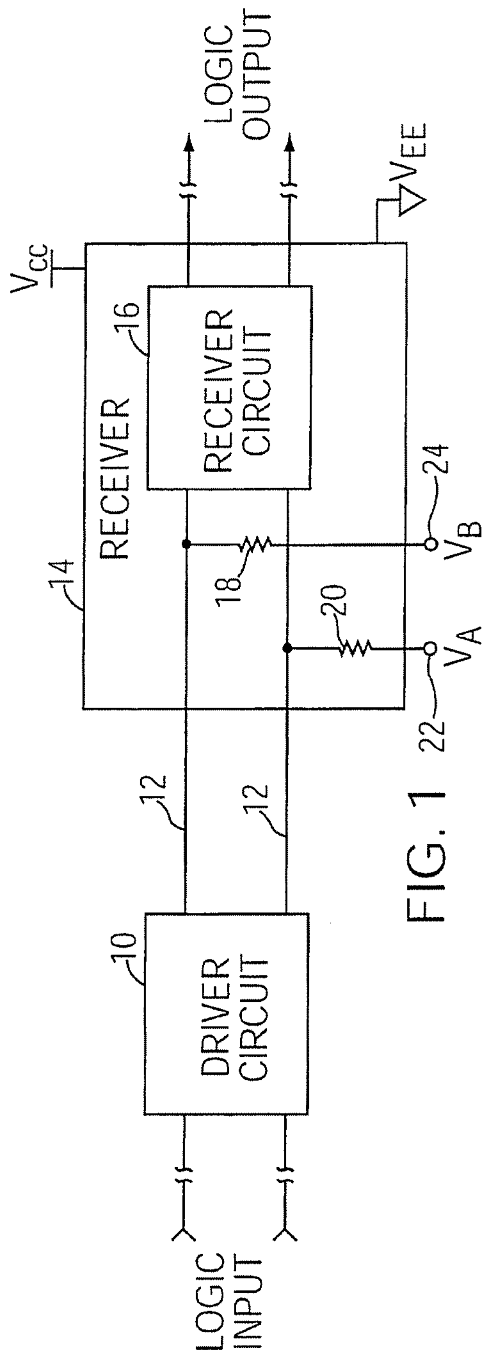

LOGIC INPUT
DRIVER CIRCUIT
10
12
12
RECEIVER
14
RECEIVER CIRCUIT
16
18
20
22
24
V_A
V_B
V_{CC}
V_{EE}
LOGIC OUTPUT

FIG. 1

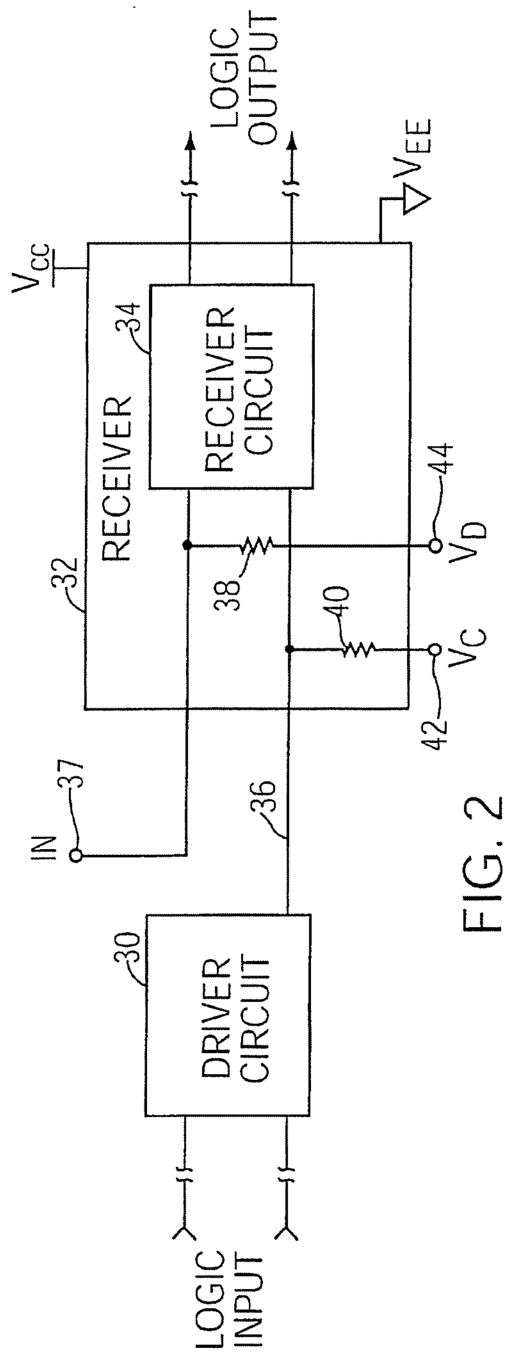

LOGIC INPUT
DRIVER CIRCUIT
30
36
IN
37
RECEIVER
32
RECEIVER CIRCUIT
34
38
40
42
44
V_C
V_D
V_{CC}
V_{EE}
LOGIC OUTPUT

FIG. 2

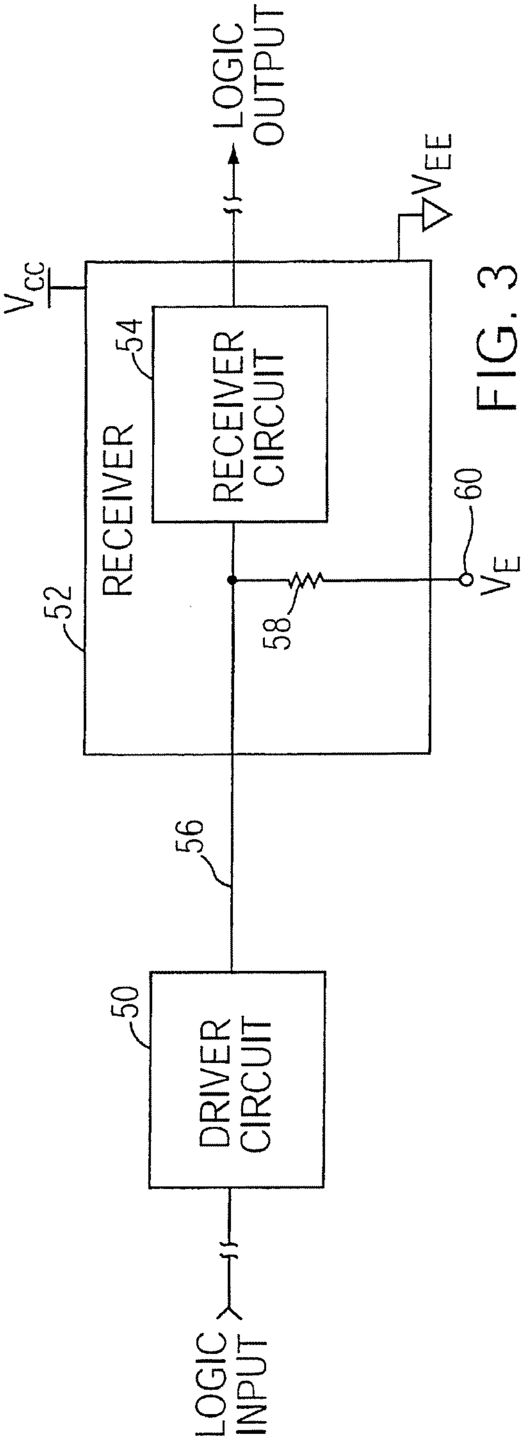

LOGIC INPUT
DRIVER CIRCUIT
50
56
52
RECEIVER
54
RECEIVER CIRCUIT
58
60
V_E
V_{CC}
V_{EE}
LOGIC OUTPUT

FIG. 3

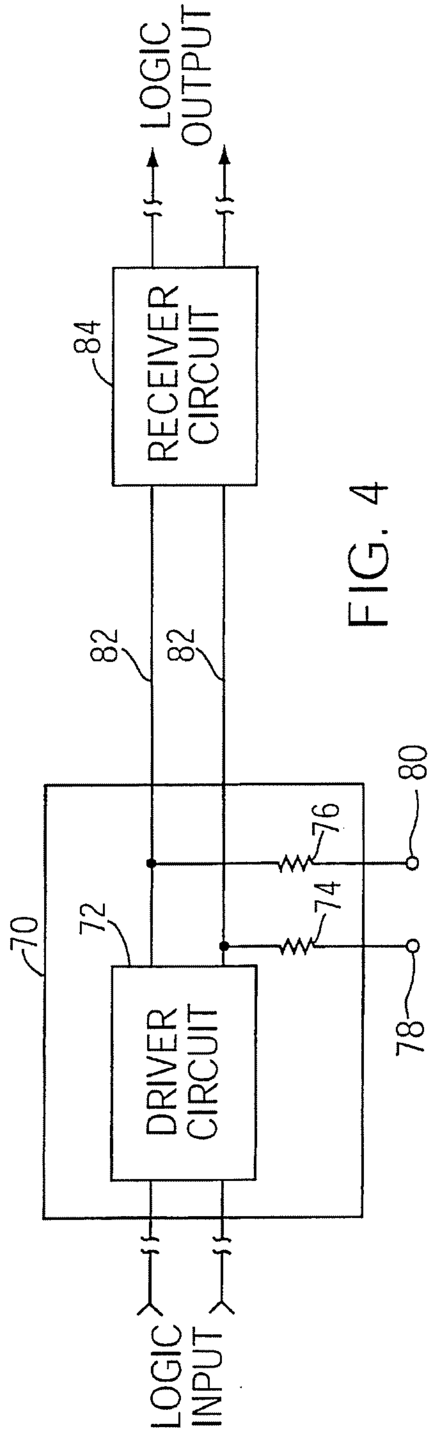
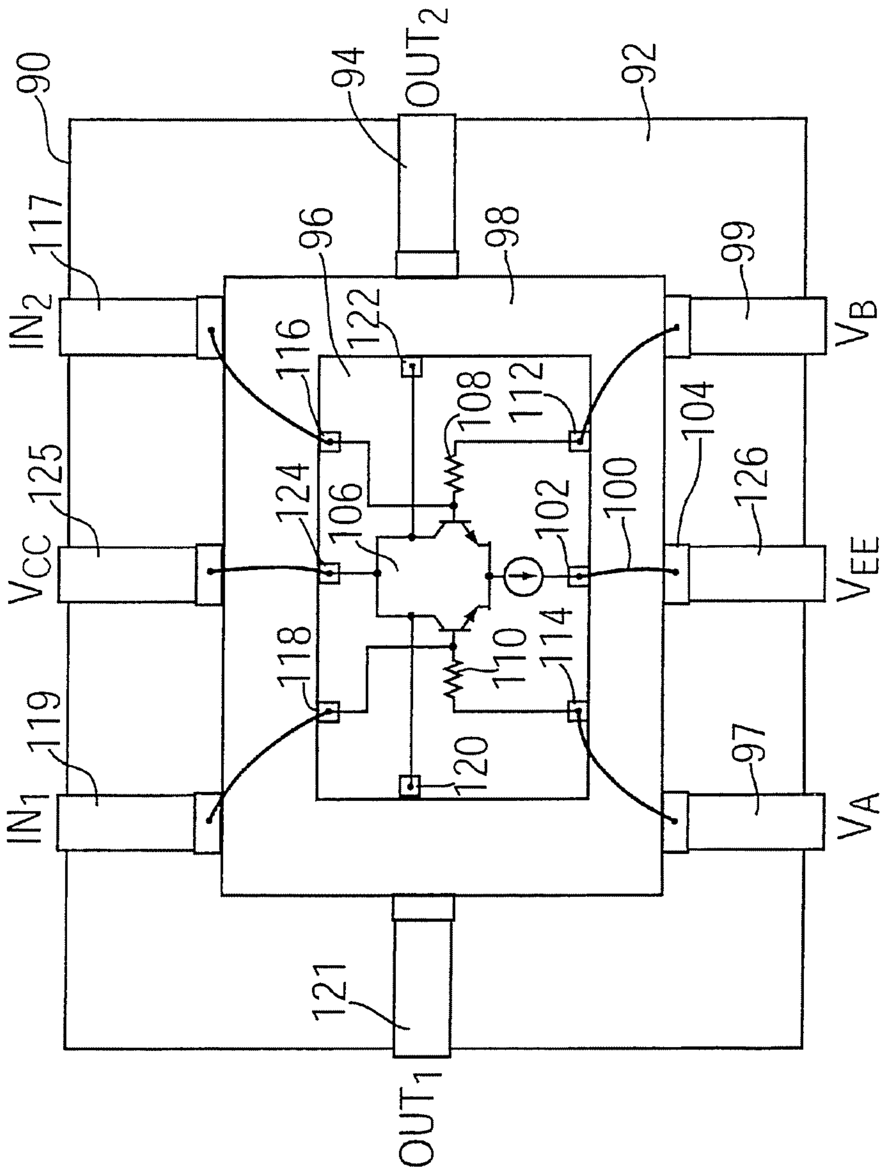

LOGIC INPUT
DRIVER CIRCUIT
70
72
74
76
78
80
82
82
84
RECEIVER CIRCUIT
LOGIC OUTPUT

FIG. 4



OUT2
OUT1
IN2
IN1
VCC
VEE
VB
VA
90
92
94
96
97
98
99
100
102
104
106
108
110
112
114
116
117
118
119
120
121
122
124
125
126

FIG. 5

PROGRAMMABLE TERMINATION FOR INTEGRATED CIRCUITS

BACKGROUND OF THE INVENTION

The present invention relates in general to electronic circuits and, more particularly, to logic circuits.

Many logic family applications have logic devices that operate within a mixed signal environment. The logic devices have logic drivers that may communicate with a logic receiver of a different logic family type. Typically, different logic family devices communicate with each other using translators to convert, for example, an ECL signal from the logic driver to a CMOS signal received at the logic receiver. A different type of translator is required for each type of logic driver and logic receiver used within the mixed signal environment. In addition, systems usually have an external termination scheme on an interconnect transmission line between the logic driver and logic receiver so the logic receiver circuit is terminated to receive the specific logic driver family type. The termination is a resistance that provides a termination for the logic device through to a voltage source Vtt. The voltage source Vtt is typically different for each logic family application. The resistance is typically chosen to equal the impedance of the interconnect transmission line to help reduce interconnect signal distortion. It is more of an advantage to have terminations as close as possible to the logic receiver circuit to help reduce interconnect signal distortion even more. Also, prior art termination schemes typically require different termination connections are used for each type of logic family device. For example, to use an ECL logic device requires a 50 ohm termination to a Vtt voltage source. A CML logic device may require termination through a resistance to a different voltage source. Most prior art logic family devices also have the termination resistors hard-wired to a circuit board making it difficult to change terminations for different logic family applications.

Hence, it is desired to have a logic receiver circuit that is programmable to allow the logic receiver circuit to communicate with different logic family driver circuits. Furthermore, it is desirable to have the terminations internal to the logic receiver circuit package so the terminations are close to the receiving circuit to help eliminate transmitted signal noise. The invention disclosed herein will address the above problems.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of a driver and receiver circuit in a differential configuration;

FIG. **2** is a schematic diagram of a driver and receiver circuit in a single-ended configuration;

FIG. **3** is a schematic diagram of a driver and receiver circuit in a modified single-ended configuration;

FIG. **4** is a schematic diagram of a driver and receiver circuit in a differential configuration with driver circuit terminations; and

FIG. **5** is a schematic diagram of a receiver circuit showing semiconductor and package connections.

DETAILED DESCRIPTION OF THE PREFERED EMBODIMENT

FIG. **1** illustrates an embodiment of a driver circuit and a receiver circuit system used in a differential configuration. The differential configuration receives a logic input signal at driver circuit **10**. Driver circuit **10** is a device from a typical

logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. The primary purpose of driver circuit **10** is to provide a signal boost for the logic input signal. At the output to driver circuit **10** is differential line **12** which transmits a differential signal from driver circuit **10** to receiver package **14**. Receiver package **14** is a semiconductor package housing receiver circuit **16**. V_{CC} and V_{EE} are power supply potentials to receiver package **14** providing power to receiver circuit **16**. Receiver circuit **16** receives a differential input signal on differential line **12** and provides a logic output signal. Receiver circuit **16** is typically a differential receiver circuit amplifier manufactured as a semiconductor die. Receiver circuit **16** and receiver package **14** are an integrated receiver circuit.

Differential line **12** is terminated with load element **18** and load element **20**. Load element **18** is connected to configuration pin **24** and load element **20** is connected to configuration pin **22**. Load elements **18, 20** are resistors contained within receiver package **14** having a resistance of 50, 75, or 100 ohms. Configuration pins **22, 24** are external pins connected to receiver package **14** and are programmable so receiver circuit **16** can communicate with different logic family drivers. To program configuration pins **22, 24**, the pins are terminated using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **16** is controlled by connecting configuration pin **22** (V_A) and configuration pin **24** (V_B) as follows.

ECL:	$V_A = V_B = V_{cc} - 2$ volts
CML:	$V_A = V_B = V_{CC}$
LVDS:	V_A connected to V_B

For example, to terminate receiver circuit **16** for an ECL application requires configuration pin **22** (V_A) and configuration pin **24** (V_B) are connected to receive configuration signal, V_{CC}−2 volts. To terminate receiver circuit **16** for an CML application requires configuration pin **22** (V_A) and configuration pin **24** (V_B) are connected to to receive configuration signal, V_{CC}. LVDS termination for receiver circuit **16** requires configuration pin **22** (V_A) and configuration pin **24** (V_B) are connected together. Termination of the configuration pins **22, 24** is done external to receiver package **14**.

FIG. **2** illustrates an embodiment of a driver circuit and a receiver circuit system used in a single-ended configuration. The single-ended configuration receives a logic input signal at driver circuit **30**. Driver circuit **30** is a device from a typical logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. Driver circuit **30** provides a signal boost for the logic input signal. Line **36** is connected to the output of driver circuit **30** to transmit a signal from driver circuit **30** to receiver package **32**. Receiver package **32** is a semiconductor package for receiver circuit **34**. V_{CC} and V_{EE} are power supply potentials to receiver package **32** providing power to receiver circuit **34**. Receiver circuit **30** is typically a differential receiver circuit amplifier manufactured as a semiconductor die. Receiver circuit **30** and receiver package **32** are an integrated receiver circuit.

Receiver circuit **34** receives two input signals: an information signal from driver circuit **30** on terminal **36**, and control signal IN on terminal **37**. Receiver circuit **34** is terminated at terminal **36** with load element **40**, and at terminal **37** with load element **38**. Load element **38** is connected to configuration pin **44** and load element **40** is connected to configuration pin **42**. Load elements **38, 40** are

resistors contained within receiver package **32** having a resistance of 50, 75, or 100 ohms. Configuration pins **42, 44** are external pins connected to receiver package **32** and are programmable so receiver circuit **34** can communicate with different logic family drivers. Configuration pins **42, 44** are programmed by terminating the pins using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **34** is controlled by connecting configuration pin **42** (V_C) and configuration pin **44** (V_D) as follows.

ECL:	$V_C = V_{CC}$ - 2 volts
	V_D = open
	IN = V_{BB}
CMOS:	V_C = open
	V_D = open
	IN = $V_{CC}/2$
TTL:	V_C = open
	V_D = open
	IN = 1.5 volts

V_{BB} is typically the middle of an output swing to an ECL output. To terminate receiver circuit **34** for an ECL application requires configuration pin **42** (V_C) is connected to receive configuration signal, V_{CC}−2, configuration pin **44** (V_D) is devoid of a configuration signal, i.e. is left open, and terminal **37** is connected to receive control signal, V_{BB}. To terminate receiver circuit **34** for a CMOS application requires configuration pin **42** (V_C) and configuration pin **44** (V_D) are devoid of a configuration signal, and terminal **37** is connected to receive control signal, $V_{CC}/2$. TTL termination for receiver circuit **34** requires configuration pin **42** (V_C) and configuration pin **44** (V_D) are devoid of a configuration signal, and terminal **37** is connected to receive control signal, 1.5 volts. Termination of the configuration pins **42, 44** is done external to receiver package **32**.

FIG. **3** illustrates an embodiment of a driver circuit and a receiver circuit system used in a modified single-ended configuration. The single-ended configuration receives a logic input signal at driver circuit **50**. Driver circuit **50** is a device from a typical type of logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. Driver circuit **50** provides a signal boost for the logic input signal. Receiver package **52** receives a drive signal on line **56** from driver circuit **50**. Receiver package **52** is a semiconductor package for receiver circuit **54**. V_{CC} and V_{EE} are power supply potentials to receiver package **52** providing power to receiver circuit **54**. Receiver circuit **54** is terminated with load element **58** which is connected to configuration pin **60**. Load element **58** is a resistor contained within receiver package **52** having a resistance of 50, 75, or 100 ohms. Configuration pin **60** is an external pin connected to receiver package **52** that is programmable so receiver circuit **54** can communicate with different logic family drivers. Configuration pin **60** is programmed by terminating the pin using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **54** is controlled by connecting configuration pin **60** (V_E) as follows.

ECL:	$V_E = V_{CC} - 2$
CML:	$V_E = V_{CC}$
LVDS:	V_E = open

To terminate receiver circuit **54** for an ECL application requires that configuration pin **60** (V_E) is connected to

receive configuration signal, V_{CC}−2. For a CML application, receiver circuit **54** is terminated with configuration pin **60** (V_E) connected to receive configuration signal, V_{CC}. LVDS termination for receiver circuit **54** requires that configuration pin **60** (V_E) be left open. Termination of the configuration pin **60** is done external to receiver package **52**.

FIG. **4** illustrates a differential configuration similar to FIG. **1**, except termination is done on driver package **70**. Driver circuit **72** is terminated at load element **74** and load element **76**. Load element **74, 76** are resistors contained within driver package **70** having a value of 50, 75, or 100 ohms. Configuration pin **78** and configuration pin **80** are configured similar to table shown for the differential configuration in FIG. **1**. Driver circuit **72** provides an output signal on differential line **82** to receiver circuit **84**.

FIG. **5** illustrates a detailed schematic of the differential configuration in FIG. **1**. Semiconductor package **90** houses a leadframe **92** with metal leads similar to lead **94** which provide input and output signals. The input and output signals consist of differential input logic signals IN_1, and IN_2, differential output logic signals OUT_1, and OUT_2, power supply signals V_{CC} and V_{EE}, and configuration signals V_A and V_B on configuration pins **97, 99** respectfully. Semiconductor die **96** is attached to flag **98** which is attached to leadframe **92**. Bond wire **100** is attached to bond pad **102** on semiconductor die **96** to provide electrical contact to bond pad **104** for the V_{EE} signal. All other input and output signals have the same bond wire configuration to provide electrical contact. The wire bonding technology used is typically a bump type technology or a ball grid array (BGA) technology. The differential configuration typically has differential amplifier **106** for receiver circuit **16** of FIG. **1**. Load elements **108, 110** are connected to bond pads **112, 114** respectfully to provide an electrical connection to configuration signals V_B and V_A. The differential signal from logic circuit **10** of FIG. **1** is received at lead **119** (IN_1) and lead **117** (IN_2) which has electrical contact to bond pads **118, 116** on semiconductor die **96**, and to differential amplifier **106**. The logic output signal from receiver circuit **16** of FIG. **1** is coupled from differential amplifier **106**, electrical contact is made to bond pads **120, 122** on semiconductor die **96**, and the signals are coupled to leads **121**. (OUT_1) and **94** (OUT_2) respectfully. Power supply is received at leads **125** (V_{CC}) and **126** (V_{EE}) making electrical contact to differential amplifier **106** through bond pads **124, 102** respectively.

An alternative method to provide termination to any of the above embodiments is to use a switch between the termination (load) elements and the (configuration) termination signals. For example, FIG. **1** has external (configuration) termination pins **22, 24** which are configured to receive different termination signals depending on the logic family application. A switch can be used to programmably connect termination pins **22, 24** to V_{CC}−2 for an ECL logic family application, or to V_{CC} for a CML logic family application. The switch can provide programmability for the termination signals to any of the previous configurations outlined herein.

Thus, a technique for generating multiple input termination options on a single integrated circuit is disclosed. A receiver circuit is programmable to configure different termination connections which allow the receiver circuit to communicate with a driver circuit from a different logic family. The receiver circuit has at least one external configuration pin that is configured to provide the necessary termination for the type of logic family driver circuit used. The configuration pin is external to a semiconductor package housing the receiver circuit. Having configuration pins external to the semiconductor package provides for easy

portability among different logic families, and easy termination options which require no additional translators to operate a mixed logic family system.

What is claimed is:

1. An integrated logic circuit having a differential input receiving a differential signal, comprising:

a receiver having first and second inputs coupled for receiving the differential signal;

a semiconductor package for housing the receiver, having first and second pins respectively coupled to the first and second inputs of the receiver, and a supply pin coupled to the receiver for providing a power supply potential;

a first termination element housed in the semiconductor package and coupled between the first input of the receiver and a first programmable configuration pin of the semiconductor package; and

a second termination element housed in the semiconductor package and coupled between the second input of the receiver and a second programmable configuration pin of the semiconductor package, wherein the first and second programmable configuration pins receive first and second termination signals to configure termination for the logic circuit.

2. The integrated logic circuit of claim **1**, wherein the first and second termination elements comprise resistors.

3. A method of configuring a receiver circuit using first and second configuration signals, and receiving first and second input signals to the receiver circuit, comprising:

coupling an information signal on the first input to the receiver circuit;

coupling a control signal on the second input to the receiver circuit;

providing a first programmable configuration pin of a semiconductor package housing the receiver circuit;

connecting a first load element between the first input of the receiver circuit and the first programmable configuration pin;

providing a second programmable configuration pin of a semiconductor package housing the receiver circuit; and

connecting a second load element between the second input of the receiver circuit and the second programmable configuration pin.

4. The method of claim **3**, wherein the first and second programmable configuration pins receive a configuration selected from the group consisting of the first configuration signal, the second configuration signal, and devoid of the first and second configuration signals.

5. The method of claim **3**, wherein the second input receives a control signal selected from the group consisting of a first control signal, a second control signal, and a third control signal.

6. An integrated circuit, comprising:

a semiconductor package having first and second pins respectively adapted for receiving first and second data signals, third and fourth pins for respectively receiving first and second termination signals, and a supply pin coupled for receiving a power supply voltage; and

a semiconductor die housed in the semiconductor package for operating from the power supply voltage, and having a first load element coupled between the first and third pins to terminate the first data signal, and a second load element coupled between the second and fourth pins to terminate the second data signal.

7. The integrated circuit of claims **6**, wherein the first and second load elements are resistors.

8. The integrated circuit of claim **6**, wherein the semiconductor die includes a receiver circuit having first and second inputs coupled to the first and second pins, respectively.

9. The integrated circuit of claim **6**, wherein the semiconductor die includes a driver circuit having first and second outputs coupled to the first and second pins, respectively.

10. The integrated circuit of claim **6**, wherein the first data signal is from a first logic family, and the third pin is coupled for receiving a first termination voltage characteristic of the first logic family.

11. The integrated circuit of claim **10**, wherein the second data signal is from a second logic family, and the fourth pin receives a second termination voltage of the second logic family.

12. A method of operating an integrated circuit, comprising the steps of:

applying first and second logic signals to first and second pins, respectively, of a semiconductor package of the integrated circuit; and

loading the first and second logic signals with first and second load elements, respectively, of the integrated circuit, where the first and second load elements are coupled to third and fourth pins of the semiconductor package to provide a programmable termination for the first and second logic signals.

13. The method of claim **12**, wherein the first and second logic signals function as a differential signal and the third and fourth pins are for coupling together to terminate the differential signal.

14. The method of claim **12**, wherein the first and second logic signals are specified in accordance with first and second logic families and the third and fourth pins are coupled to first and second configuration signals of the first and second logic families, respectively.

15. The method of claims **14**, wherein the first and second logic signals are ECL signals referenced to a supply voltage, and the first and second configuration signals have values equal to the supply voltage minus about two volts.

16. The integrated logic circuit of claim **12**, further comprising the step of applying a power supply voltage to a fifth pin of the semiconductor package to bias the integrated circuit.

* * * * *

EXHIBIT C

US005361001A

United States Patent [19]

Stolfa

[11] **Patent Number:** **5,361,001**

[45] **Date of Patent:** **Nov. 1, 1994**

[54] **CIRCUIT AND METHOD OF PREVIEWING ANALOG TRIMMING**

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[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **160,762**

[22] Filed: **Dec. 3, 1993**

[51] **Int. Cl.**[5] **H03K 3/01**; H03B 1/04

[52] **U.S. Cl.** **327/530**; 327/525; 327/312

[58] **Field of Search** 307/202.1, 296.1, 547, 307/548

[56] **References Cited**

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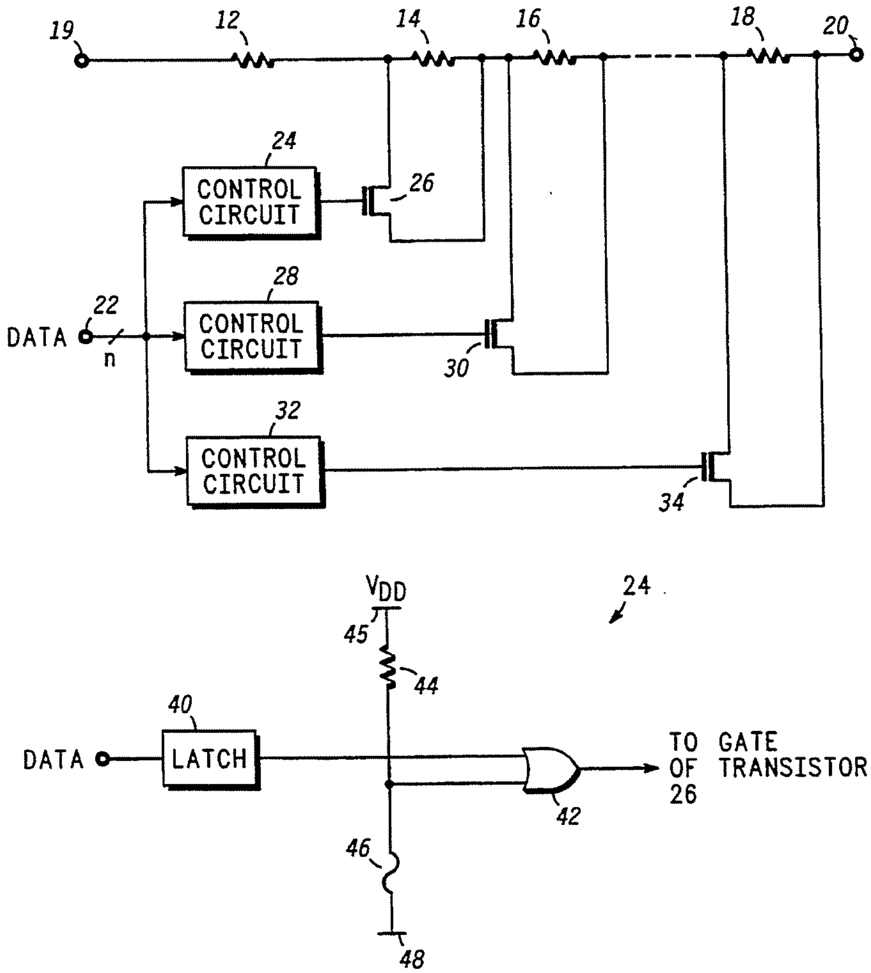
0262716 10/1990 Japan 307/202.1

Primary Examiner—Margaret Rose Wambach
Attorney, Agent, or Firm—Robert D. Atkins

[57] **ABSTRACT**

An analog trim circuit enables and disables one or more serially connected passive elements for setting characteristics of the circuit. Each passive element has a transistor across its first and second conduction terminals operating in response to a control signal from a control circuit for enabling and disabling conduction through the associated passive element. The control circuits are responsive to a data signal for providing the control signals that enable and disable the conduction through the passive elements. The data signal allows a preview of the trimming results. The fuse in certain ones of the control circuits are blown to set the control signals to fixed values after removal of the data signal.

7 Claims, 1 Drawing Sheet



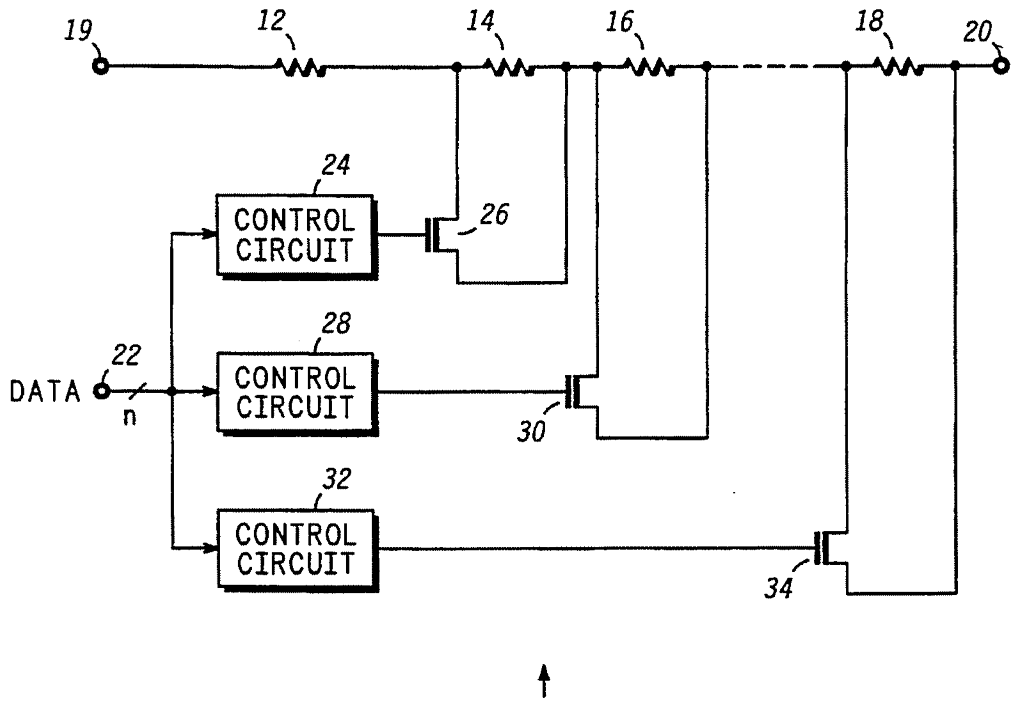
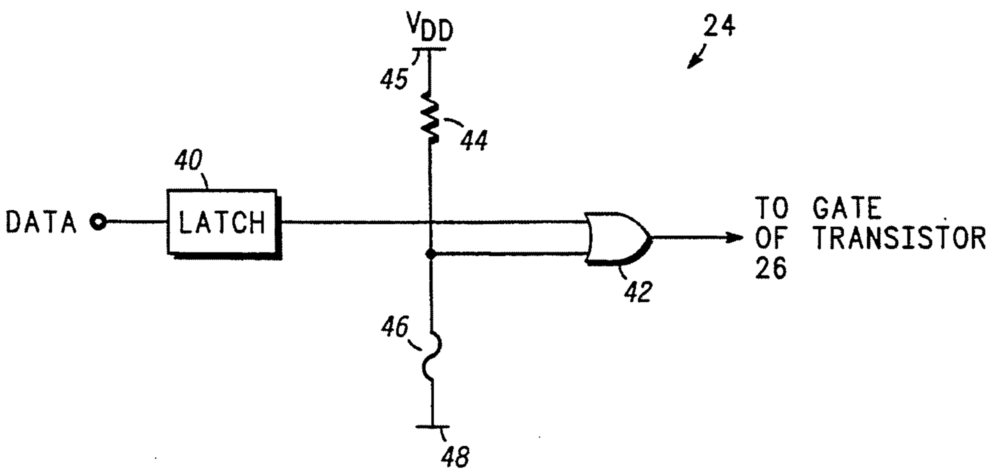

19
12
14
16
18
20
24
CONTROL CIRCUIT
26
28
DATA
22
n
CONTROL CIRCUIT
30
32
CONTROL CIRCUIT
34
10

FIG. 1

FIG. 2


V_{DD}
24
45
44
40
DATA
LATCH
TO GATE OF TRANSISTOR 26
42
46
48

CIRCUIT AND METHOD OF PREVIEWING ANALOG TRIMMING

BACKGROUND OF THE INVENTION

The present invention relates in general to analog trim circuits and, more particularly, to a technique of previewing the analog trim results before blowing a fuse to lock the trim in place.

In manufacturing analog integrated circuits, the basic building blocks are usually not accurately controlled by the manufacturing process as may be desired. For example, capacitors and resistors may have the wrong value, and MOS transistors may have the wrong gain setting. There are too many variables in the manufacturing process to yield absolute predictable results. Yet historically analog circuits often require very accurate voltage references, frequency references, and accurately ratioed elements.

To compensate for the process variability, many electronic circuits use analog trimming during test to set resistor values as necessary for proper operation of the circuit. A typical trimming technique utilizes a resistor ladder comprising a series of serially coupled resistors each in parallel with either a fuse or anti-fuse. A fuse is a device that is substantially an electrical short until it is blown open. An anti-fuse is an electrical open until blown when it becomes substantially an electrical short.

The fuse-blowing approach may take several forms, each with its own shortcomings. Laser fuses may be used directly across each resistor element in the ladder to enable and disable conduction through the resistor. During test, certain resistors are selected to open the shunt element thereby adding resistance to the serial path. The resistor ladder should be adjustable at wafer test over a range from say 10 to 2,560 ohms in 10 ohm increments.

The analog trimming may be performed iteratively, i.e. test, trim, test, trim, to measure the effect of the course trim and determine the necessary fine trimming. For iterative trimming, a laser trim system is typically installed on the wafer tester to alternately test and trim. However, one laser system per tester is very expensive. The laser is often in an idle state waiting for the tester. Moreover, if either the test system or laser breaks down both are inoperative.

An alternate approach is to use a zener anti-fuse across the resistor ladder. Such an element can be cheaply trimmed on the tester so that iterative testing can be done in one pass on the tester. Zener anti-fuses require large currents to program. Therefore, each anti-fuse requires its own external pad and probe card needle. This restricts the programming bit count to say 5–10 bits before the die area for test pads and complexity of the probe card requirements become prohibitive.

In general, iterative testing is a slow and expensive process. Consequently, many trimming techniques utilize only a single pass to evaluate which resistors in the serial string should be included to achieve the desired analog circuit operation. Thus, as result of a test measurement, the user blows the shunt fuse elements whereby the circuit is expected to operate as planned. The process of blowing the fuses typically involves laser trimming off-line from the test set to cut the poly material and open the shunt element. The circuit may be returned to the test set to verify proper trimming. If the subsequent testing should fail, the part is typically discarded since it is difficult to patch the shunt fuse elements.

Hence, a need exists for an iterative trimming to evaluate the results of test before permanently setting the trim.

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a block diagram illustrating an analog trimming circuit; and

FIG. **2** is a schematic diagram illustrating the control circuit of FIG. **1**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

An analog trim circuit is shown in FIG. **1** including a passive ladder network **10** comprising resistors **12**, **14**, **16** and **18** serially coupled between terminal **19** and terminal **20**. Resistor **12** is non-trimmable and provides the minimum ladder resistance (R_{MIN}). Resistors **14–18** are selected in an exponential series, such as 1280, 640, 320, 160, 80, 40, 20, and 10 ohms. Resistors **14–18** are passive elements each with first and second conduction terminals. Other passive elements may also be used in the trim circuit. A data signal is applied at terminal **22**. One bit of the data signal is applied to each of control circuits **20**, **28** and **32**. An address signal selects the control circuit to latch one bit of the data signal.

Control circuit **24** provides a control signal to the gate of MOS transistor **26**. The drain and source of transistor **26** are coupled to first and second conduction terminals of resistor **14**. Likewise, control circuit **28** provides a control signal to the gate of MOS transistor **30** which has its drain and source coupled across resistor **16**. Control circuit **32** provides a control signal to the gate of MOS transistor **34**. The drain and source of transistor **34** are coupled across the first and second conduction terminals of resistor **18**. The effective resistance through resistor ladder **10** is thus temporarily set by transistors **26**, **30** and **34** selectively enabling and disabling conduction through resistors **14–18** upon receiving a high state or low state of control signals from control circuits **24**, **28** and **32**. With the above trimming scheme, the resistor ladder is controllable from R_{MIN} to R_{MIN}+2,560 ohms assuming eight trimmable resistors in 256 possible 10 ohm increments.

Turning to FIG. **2**, further detail of control circuit **24** is shown. Control circuits **28** and **32** follow a similar construction and operation as described for control circuit **24**. The data signal is latched in latching circuit **40** for application to a first input of OR gate **42**. An address signal enables latching circuit **40** to latch the data bit. Resistor **44** is coupled between the second input of OR gate **42** and power supply conductor **45**. Power supply conductor **45** operates at a positive potential VDD such as 5 volts. Fuse **46** is coupled between the second input of OR gate **42** and power supply conductor **48** operating at ground potential. The output of OR gate **42** provides the control signal to the gate of transistor **26**. An alternate embodiment of control circuit **24** may replace OR gate **42** with a NAND gate while resistor **44** and fuse **46** exchange places in the circuit.

Trim circuits are used in a variety of applications. For example, a circuit may require a given frequency f_o determined by an RC time constant such that the frequency is inversely proportional to RC. The resistance R and capacitance C should be selected such that the nominal process target values of sheet ρ (resistance per

unit area) and capacitance per unit area yield the desired frequency f_o. However, the actual process values of resistance and capacitance may vary by 5%–10%. Thus, the trimmable resistor ladder **10** must be trimmed to compensate for any variation in sheet ρ and capacitance per unit area.

During testing at wafer level, the circuit under test is exercised and any correction necessary to resistor ladder **10** is calculated by a binary search. Steps are taken to determine whether a resistor should be trimmed such that it is in the upper half or lower half of its trimmable range, i.e. determining if the most significant bit or largest resistor should be shorted or left to remain in resistor ladder **10**. With resistor ladder **10** trimmed to its most significant bit the circuit under test is again tested and a correction is calculated to determine if it should be trimmed to the upper half or lower half of the remaining trimmable range. As a result, the next most significant resistor is shorted or allowed to remain. The process continues until all trimmable resistors have been checked.

Consider the trimming operation during test where a logic one data signal is stored in latching circuit **40** of each of control circuits **24**, **28** and **32**. The output of each OR gate **42** goes high and enables transistors **26**, **30** and **34**. Resistors **14–18** are substantially shorted, i.e. disabling the conduction path through resistors **14–18**. The resistance of ladder **10** is equal to R_{MIN}.

To perform trim preview during test, the data signal to control circuit **24** is set to logic zero and stored in its latching circuit **40**. At wafer test all fuses are yet unblown so that all fuse inputs to the OR-gates are low. The control signal at the output of OR-gate **42** goes low and turns off transistor **26** to enable the conduction through resistor **14**. The resistance of ladder **10** increases to $R_{MIN}+R_{14}$, where R_{14} is the value of resistor **14**. The effect of the added resistance on the operation of the circuit under test may be checked and verified by the tester. If more resistance is needed, the data signal to control circuit **28** may be set to logic zero. The control signal to transistor **30** goes low as described above for control circuit **24**. Transistor **30** turns off and enables the conduction through resistor **16**. The resistance of ladder **10** increases to $R_{MIN}+R_{14}+R_{16}$, where R_{16} is the value of resistor **16**. Again, the effect of the added resistance on the operation of the circuit under test may be checked and verified by the tester. The process continues until the circuit under test operates as desired. Note at this point, the trimming process is temporary and dependent on the data signals to control circuits **24**, **28** and **32**. No fuses have yet been blown to lock in the trim. Thus, different combinations of resistors **14–18** may be previewed and checked to achieve optimal results.

An alternate trim approach could initially set the data signals to logic zero in control circuits **24**, **28** and **32**. The output of each OR gate **42** goes low and disables transistors **26**, **30** and **34**. The shunt elements **26**, **30** and **34** are substantially opened, i.e. enabling conduction through resistors **14–18**, thereby making ladder **10** resistance maximum. The testing preview involves setting the data signals to logic one and iteratively enabling transistors **26**, **30** and **34** to disable conduction through resistors **14–18** and reduce resistance in ladder **10**. The process continues until the circuit under test operates as desired. Again, the trimming process is temporary and dependent on the data signals to control circuits **24**, **28** and **32**. No fuses have yet been blown to lock in the trim. Different combinations of resistors **14–18** may be tried and checked to achieve optimal results.

Another embodiment of the present invention is to configure the resistor ladder with the resistors in parallel and the control transistors in series with each resistor.

For the circuits under test that functionally pass, the bit pattern of trim is recorded in a file by wafer and die site. The file accompanies the wafer to a laser fuse system where the selected fuses **46** are blown. Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore the permanent trim. The control signals from control circuits **24**, **28** and **32** are thus set to a fixed value by blowing the selected fuses **46** in the control circuits after removal of the data signal at terminal **22**.

The fuses are generally doped polycrystalline silicon films sometimes silicided polycrystalline silicon films in the range of 10 to 500 ohms. The polysilicon film is usually made in the shape of a polysilicon resistor with a width five to ten times its length. The ends of the fuses are connected by metal interconnects to the relevant circuitry. The fuse usually has most or all overlying oxide layers removed. With the use of on-die alignment marks the laser beam of approximately 1 μm–2 μm beam width is focused on the center of the fuse. The laser beam is a pulsed signal of such an energy that the polysilicon is vaporized and the fuse is severed and therefore permanently no longer conductive.

A key feature of the present invention is to preview trimming at wafer test to provide an economical means of iteratively trimming the resistive ladder using data provided by the tester. A data signal selectively trims the resistor ladder. The trimming is temporary and may be modified with different data signals to achieve optimal results. When the proper pattern of trim bits is determined for each individual circuit under test, that data is recorded and transferred off-line to the laser trimmer along with the wafer. The laser trim system blows the appropriate fuses for each circuit under test according to the pattern previously determined by testing various trimming options. Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore sets the permanent trim. The preview trimming process allows optimization of the bit pattern for trimming before the actual laser trimming. Furthermore, the testing and the fusing systems may remain separate without requiring multiple passes through each.

While specific embodiments of the present invention have been shown and described, further modifications and improvements will occur to those skilled in the art. It is understood that the invention is not limited to the particular forms shown and it is intended for the appended claims to cover all modifications which do not depart from the spirit and scope of this invention.

I claim:

1. An analog trim circuit, comprising:

a passive element having first and second conduction terminals;

first means coupled across said passive element and operating in response to a control signal for enabling and disabling conduction through said passive element, said first means includes a transistor having a gate, a drain and a source, said drain being coupled to said first conduction terminal, said

source being coupled to said second conduction terminal, said gate being coupled for receiving said control signal; and

second means responsive to a data signal for providing said control signal to said first means to enable and disable said conduction through said passive element, said second means setting said control signal to a fixed value after removal of said data signal.

2. The analog trim circuit of claim 1 wherein said passive element includes a first resistor coupled between said first and second conduction terminals.

3. The analog trim circuit of claim 2 wherein said second means includes:

a latching circuit having an input coupled for receiving said data signal and having an output;

a logic gate having first and second inputs and an output, said first input being coupled to said output of said latching circuit, said output being coupled for providing said control signal;

a second resistor coupled between a first power supply conductor and said second input of said logic gate; and

a fuse coupled between said second input of said logic gate and a second power supply conductor.

4. A method of analog trimming, comprising the steps of:

enabling conduction through a passive element in response to a first state of a control signal;

disabling conduction through said passive element in response to a second state of said control signal;

activating said control signal in response to a data signal to enable and disable said conduction

through said passive element, said activating step including the steps

(a) latching said data signal, and

(b) logically combining said data signal with a logic signal for providing said control signal; and

setting said control signal to a fixed value after removal of said data signal.

5. The method of claim 4 wherein said setting step includes the steps of:

removing said data signal; and

blowing a fuse to set said control signal at said fixed value.

6. An analog trim circuit, comprising:

a passive element having first and second conduction terminals;

a transistor having a gate, a drain and a source, said drain being coupled to said first conduction terminal, said source being coupled to said second conduction terminal, said gate being coupled for receiving a control signal;

a latching circuit having an input coupled for receiving a data signal and having an output;

a logic gate having first and second inputs and an output, said first input being coupled to said output of said latching circuit, said output being coupled for providing said control signal;

a first resistor coupled between a first power supply conductor and said second input of said logic gate; and

a fuse coupled between said second input of said logic gate and a second power supply conductor.

7. The analog trim circuit of claim 6 wherein said passive element includes a first resistor coupled between said first and second conduction terminals.

* * * * *

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(Except In U.S. Plaintiff Cases)

County Of Residence Of First Listed Defendant:
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(c) Attorneys (Firm Name, Address, And Telephone Number)
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John W. Shaw, Esquire (#3362)
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(302) 571-6600

Attorneys (If Known)

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☐ 345 Marine Product Liability
☐ 350 Motor Vehicle
☐ 355 Motor Vehicle Product Liability
☐ 360 Other Personal Injury

PERSONAL INJURY
☐ 362 Personal Injury - Med Malpractice
☐ 365 Personal Injury - Product Liability
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PERSONAL ROPERTY
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☐ 371 Truth in Lending
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☐ 535 Death Penalty
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☐ 555 Prison Condition

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☐ 690 Other

LABOR
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☐ 720 Labor/Mgmt Relations
☐ 730 Labor/Mgmt. Reporting & Disclosure Act
☐ 740 Railway Labor Act
☐ 790 Other Labor Litigation
☐ 791 Empl Ret Inc Security Act

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☐ 422 Appeal 28 U.S.C. 158
☐ 423 Withdrawal 28 U.S.C. 157

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☐ 864 SSID Title XVI
☐ 865 RSI (405(g))

FEDERAL TAX SUITS
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☐ 850 Securities/Commodities/ Exchange
☐ 875 Customer Challenge 12 U.S.C. 3410
☐ 891 Agricultural Acts
☐ 892 Economic Stabilization Act
☐ 893 Environmental Matters
☐ 894 Energy Allocation Act
☐ 895 Freedom of Information Act
☐ 900 Appeal of Fee Determination Under Equal Access to Justice
☐ 950 Constitutionality of State Statutes
☐ 890 Other Statutory Actions

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☐ 7 Appeal to District Judge from Magistrate Judgment

VI. CAUSE OF ACTION
(CITE THE U.S. CIVIL STATUTE UNDER WHICH YOU ARE FILING AND WRITE BRIEF STATEMENT OF CAUSE DO NOT CITE JURISDICTIONAL STATUTSE UNLESS DIVERSITY.):
28 U.S.C. §2201 et, seq.; 35 U.S.C. § 101 et seq.

Brief description of cause:
Cause of action for declaratory judgment of noninfringement and invalidity.

VII. REQUESTED IN COMPLAINT: ☐ CHECK IF THIS IS A UNDER F.R.C.P. 23 **CLASS ACTION** ☐ YES ☐ NO **DEMAND** $
Check YES only if demanded in complaint
JURY DEMAND: ☒ YES ☐ NO

VIII. RELATED CASE(S) (See instructions) **IF ANY** JUDGE: DOCKET NUMBER:

DATE 11/30/06 SIGNATURE OF ATTORNEY OF RECORD John W. Shaw by Andrew A. Lundgren

FOR OFFICE USE ONLY

RECEIPT # ____ AMOUNT ____ APPLYING IFP ____ JUDGE ____ MAG. JUDGE ____

INSTRUCTIONS FOR ATTORNEYS COMPLETING CIVIL COVER SHEET FORM JS-44

Authority For Civil Cover Sheet

The JS-44 civil cover sheet and the information contained herein neither replaces nor supplements the filings and service of pleading or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. Consequently a civil cover sheet is submitted to the Clerk of Court for each civil complaint filed. The attorney filing a case should complete the form as follows:

I. (a) **Plaintiffs - Defendants.** Enter names (last, first, middle initial) of plaintiff and defendant. If the plaintiff or defendant is a government agency, use only the full name or standard abbreviations. If the plaintiff or defendant is an official within a government agency, identify first the agency and then the official, giving both name and title.

(b) **County of Residence.** For each civil case filed, except U.S. plaintiff cases, enter the name of the county where the first listed plaintiff resides at the time of filing. In U.S. plaintiff cases, enter the name of the county in which the first listed defendant resides at the time of filing. (NOTE: In land condemnation cases, the county of residence of the "defendant" is the location of the tract of land involved).

(c) **Attorneys.** Enter firm name, address, telephone number, and attorney of record. If there are several attorneys, list them on an attachment, noting in this section "(see attachment)."

II. **Jurisdiction.** The basis of jurisdiction is set forth under Rule 8(a), F.R.C.P., which requires that jurisdictions be shown in pleadings. Place an "X" in one of the boxes. If there is more than one basis of jurisdiction, precedence is given in the order shown below.

United States plaintiff. (1) Jurisdiction is based on 28 U.S.C. 1345 and 1348. Suits by agencies and officers of the United States are included here.

United States defendant. (2) When the plaintiff is suing the United States, its officers or agencies, place an "X" in this box.

Federal question. (3) This refers to suits under 28 U.S.C. 1331, where jurisdiction arises under the Constitution of the United States, an amendment to the Constitution, an act of Congress or a treaty of the United States. In cases where the U.S. is a party, the U.S. plaintiff or defendant code takes precedence, and box 1 or 2 should be marked.

Diversity of citizenship. (4) This refers to suits under 28 U.S.C. 1332, where parties are citizens of different states. When Box 4 is checked, the citizenship of the different parties must be checked. (See Section III below; federal question actions take precedence over diversity cases.)

III. **Residence (citizenship) of Principal Parties.** This section of the JS-44 is to be completed if diversity of citizenship was indicated above. Mark this section for each principal party.

IV. **Cause of Action.** Report the civil statute directly related to the cause of action and give a brief description of the cause.

V. **Nature of Suit.** Place an "X" in the appropriate box. If the nature of suit cannot be determined, be sure the cause of action, in Section IV above, is sufficient to enable the deputy clerk or the statistical clerks in the Administrative Office to determine the nature of suit. If the cause fits more than one nature of suit, select the most definitive.

VI. **Origin.** Place an "X" in one of the seven boxes.

Original Proceedings. (1) Cases which originate in the United States district courts.

Removed from State Court. (2) Proceedings initiated in state courts may be removed to the district courts under Title 28 U.S.C. Section 1441. When the petition for removal is granted, check this box.

Remanded from Appellate Court. (3) Check this box for cases remanded to the district court for further action. Use the date of remand as the filing date.

Reinstated or Reopened. (4) Check this box for cases reinstated or reopened in the district court. Use the reopening date as the filing date.

Transferred from Another District. (5) For cases transferred under Title 28 U.S.C. Section 1404(a). Do not use this for within district transfers or multidistrict litigation transfers.

Multidistrict Litigation. (6) Check this box when a multidistrict case is transferred into the district under authority of title 28 U.S.C. Section 1407. When this box is checked, do not check (5) above.

Appeal to District Judge from Magistrate Judgment. (7) Check this box for an appeal from a magistrate's decision.

VII. **Requested in Complaint.** Class Action. Place an "X" in this box if you are filing a class action under Rule 23, F.R.Cv.P.

Demand. In this space enter the dollar amount (in thousands of dollars) being demanded or indicate other demand such as a preliminary injunction.

Jury Demand. Check the appropriate box to indicate whether or not a jury is being demanded.

VIII. **Related Cases.** This section of the JS-44 is used to reference relating pending cases if any. If there are related pending cases, insert the docket numbers and the corresponding judge names for such cases.

Date and Attorney Signature. Date and sign the civil cover sheet.

AO FORM 85 RECEIPT (REV. 9/04)

United States District Court for the District of Delaware

Civil Action No. 06 - 720

ACKNOWLEDGMENT OF RECEIPT FOR AO FORM 85

NOTICE OF AVAILABILITY OF A UNITED STATES MAGISTRATE JUDGE TO EXERCISE JURISDICTION

I HEREBY ACKNOWLEDGE RECEIPT OF 2 COPIES OF AO FORM 85.

NOV 30 2006
(Date forms issued)

(Signature of Party or their Representative)

JASON SPARKLIN
(Printed name of Party or their Representative)

Note: Completed receipt will be filed in the Civil Action